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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,428	12/28/2001	William H. Moody II	CROSS1510	1923

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,428	MOODY, WILLIAM H.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-37,42-48 and 53-58* is/are rejected.

7)☒ Claim(s) *38-41,49-52 and 56-58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 20, 2004 has been entered.

2. Claims 1-29 have been cancelled; new claims 30-58 have been added.

3. Applicant's arguments with respect to claims 30-58 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 31, 35, 36, 43, 46 and 47 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claims 31 and 43, the specification teaches connecting a first component to a second component, and then, based upon a comparison, operating the second component, "either with or without the first component" (fig. 1; paragraph 19). The second component appears to correspond to the subsequently described primary system (fig. 2; paragraph 20), since both

operate with or without the other component after a comparison. However, the secondary component in the claim is not the primary component.

As per claims 35 and 46, the specification describes memories for storing identifiers (fig. 2, memories 12 and 14; fig. 4, memories 31-33), but does not teach these memories be used solely used for storing identifiers. There is no express restriction on storing other information.

As per claims 36 and 47, the specification describes memories (fig. 2, memories 12 and 14; fig. 4, memories 31-33) that are non-volatile (paragraphs 16, 17, 21 and 26), but does not expressly teach these memories to be EEPROMS.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 30, 32-35, 37, 42, 45, 46, 48 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghori et al., U.S. Patent No. 5,884,901 ("Ghori"), in view of Dreyer et al., U.S. Patent No. 5,790,834 ("Dreyer").

As per claim 30, Ghori teaches a method comprising:

providing a primary electronic component having a first identifier, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, oem cpu; col. 5, lines 29-38, oem cpu family is compared to upgrade family, indicating that the first identifier exists);

providing a secondary electronic component having a second identifier stored therein, wherein the second identifier includes branding information corresponding to the secondary electronic component (fig. 2, upgrade processor stores upgrade_id; fig. 3, upgrade_id includes family);

coupling the secondary component to the primary component (fig. 1, upgrade processor inserted in upgrade socket);

comparing the first identifier to the second identifier (col. 5, lines 29-38, oem cpu family is compared to upgrade family);

operating the primary component in conjunction with the secondary component if the first identifier is compatible with the second identifier (col. 5, lines 14-17 and 38-40); and

operating the primary component without the secondary component if the first identifier is not compatible with the second identifier (col. 5, lines 48-54).

However, Ghori does not expressly teach the storing the first identifier in the primary component. Dreyer teaches the details of storing a first identifier within a primary component, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, information 31 includes family field 32; col. 6, lines 5-19). Ghori and Dreyer are analogous art because they are from the same field of endeavor involving the use of identifiers in electronic components. At the time of the invention, it would have been obvious to one or ordinary skill in the art to apply Dreyer's details of storing a first identifier to Ghori's primary component. A motivation for doing so would have been to ensure the integrity of Ghori's method.

As per claim 32, Ghori teaches compatible is matching or identical (col. 5, lines 29-38).

As per claim 33, Dreyer teaches storing the first identifier in a memory in the primary component (col. 5, lines 51-67). Ghori teaches storing the second identifier in a memory in the secondary component (fig. 3, family stored in bits 0-3).

As per claim 34, Dreyer teaches storing an identifier in nonvolatile memory (col. 5, lines 51-67). Ghori also teaches storing an identifier in nonvolatile memory (col. 4, lines 53-61).

As per claim 35, Ghori teaches the non-volatile memory in the second component is used solely for storing the second identifier (fig. 3, family stored in bits 0-3; col. 4, line 62 – col. 5, line 12).

As per claim 37, Ghori teaches coupling the secondary component to the primary component comprises coupling the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the non-volatile memory and the primary component for the purposes of comparing the first identifier to the second identifier (fig. 1, private bus 40 and buses 13 or 83; col. 3, line 59 – col. 4, line 16).

As per claim 42, Ghori teaches a system comprising:

a primary component having a first identifier, wherein the first identifier includes branding information corresponding to the primary component (fig. 1, oem cpu; col. 5, lines 29-38, oem cpu family is compared to upgrade family, indicating that the first identifier exists); and

a secondary component having a second memory, wherein the second memory has a second identifier stored therein and the second identifier includes branding information

corresponding to the secondary component (fig. 2, upgrade processor stores upgrade_id; fig. 3, upgrade_id includes family);

wherein the secondary component is configured to be coupled to the primary component (fig. 1, upgrade processor coupled via upgrade socket);;

wherein the primary component is configured to compare the first identifier to the second identifier (col. 5, lines 29-38, oem cpu executes comparison by operating system);

wherein the primary component is configured to enable operation in conjunction with the secondary component if the first identifier is compatible with the second identifier (col. 5, lines 14-17 and 38-40) and operate without the secondary component if the first identifier is not compatible with the second identifier (col. 5, lines 48-54).

However, Ghori does not expressly teach the primary component having a first memory for storing the first identifier. Dreyer teaches the details of storing a first identifier in first memory of a primary component, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, information 31 includes family field 32; col. 5, lines 51-67; col. 6, lines 5-19). Ghori and Dreyer are analogous art because they are from the same field of endeavor involving the use of identifiers in electronic components. At the time of the invention, it would have been obvious to one or ordinary skill in the art to apply Dreyer's details of storing a first identifier to Ghori's primary component. A motivation for doing so would have been to ensure the integrity of Ghori's system.

As per claim 45, Dreyer teaches storing an identifier in nonvolatile memory (col. 5, lines 51-67). Ghori also teaches storing an identifier in nonvolatile memory (col. 4, lines 53-61).

As per claim 46, Ghori teaches the non-volatile memory in the second component is used solely for storing the second identifier (fig. 3, family stored in bits 0-3; col. 4, line 62 – col. 5, line 12).

As per claim 48, Ghori teaches coupling the secondary component to the primary component comprises coupling the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the non-volatile memory and the primary component for the purposes of comparing the first identifier to the second identifier (fig. 1, private bus 40 and buses 13 or 83; col. 3, line 59 – col. 4, line 16).

As per claim 53, Ghori teaches an electrical component configured to have a secondary component coupled thereto (fig. 1, computer system coupled to upgrade processor), wherein the electrical component comprises:

a functional portion (fig.1, cache 11);

an interface configured to couple the functional portion to a secondary component (fig. 1, bus 13);

a first identifier includes branding information corresponding to the electrical component (col. 5, lines 29-38, oem cpu family is compared to upgrade family, indicating that the first identifier exists); and

a comparator configured to receive a second identifier (fig. 1, oem cpu; col. 5, lines 29-38, oem cpu receives upgrade_id), including branding information corresponding to the second

component (fig. 2, upgrade processor stores upgrade_id; fig. 3, upgrade_id includes family), from the secondary component and to compare the first identifier to the second identifier (col. 5, lines 29-38, oem cpu executes comparison by operating system), wherein the comparator is configured to enable operation in conjunction with the secondary component if the first identifier is compatible with the second identifier and operate without the secondary component if the first identifier is not compatible with the second identifier (col. 5, lines 14-17, 38-40 & 48-54).

However, Ghori does not expressly teach the electrical component having a first memory for storing the first identifier. Dreyer teaches the details of storing a first identifier in first memory of an electrical component, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, information 31 includes family field 32; col. 5, lines 51-67; col. 6, lines 5-19). Ghori and Dreyer are analogous art because they are from the same field of endeavor involving the use of identifiers in electronic components. At the time of the invention, it would have been obvious to one or ordinary skill in the art to apply Dreyer's details of storing a first identifier to Ghori's electrical component. A motivation for doing so would have been to ensure the integrity of Ghori's system.

As per claim 54, Dreyer teaches storing an identifier in nonvolatile memory (col. 5, lines 51-67).

As per claim 55, Ghori's cache does not utilize memory of the oem cpu.

Allowable Subject Matter

6. Claims 38-41, 49-52 and 56-58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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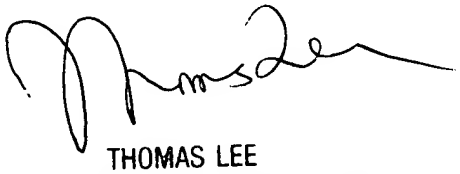
March 8, 2005



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